REMARKS

In response to the Office Action dated August 28, 2008, Applicants respectfully request reconsideration and withdrawal of the objections to the disclosure and claims, and the rejection of the claims.

The drawings were objected to as not showing every feature specified in the claims, and for containing blocks that were not labeled to indicate the structure that they represent. In response thereto, a replacement sheet of drawings is being submitted herewith, in which the sole figure has been revised as requested by the examiner, to address the objections.

The specification was objected to on the grounds that the reference symbol "CR" was used to identify both an encryption means and a security module. The Office Action refers to the paragraph on page 3, lines 18-19, of the specification as using "CR" to designate the encryption means. However, it is to be noted that this paragraph was deleted in the Preliminary Amendment filed September 23, 2005. As amended, the specification only uses the symbol "CR" to identify the security module. The examiner is respectfully requested to confirm that the amendments submitted with the filing of the application papers have been properly entered into the record, and to withdraw the objection.

The Office Action contains an objection to claim 1 as containing an informality. It is noted that claim 1 was canceled in the Preliminary Amendment filed concurrently with the application documents on September 23, 2005, and it appears that the examiner meant to refer to claim 9. In any event, claim 9 has been canceled, rendering the basis for the objection moot.

Claims 9-14 were rejected under 35 U.S.C. § 102, on the basis of the Ma et al patent (US 6,996,725). To clarify the scope of the subject matter upon which Applicants are believed to be entitled to obtain protection, claims 9-11 have been canceled, and new claims 15-16 are being presented herein. Claims 12-16 are pending, with claim 15 being the sole independent claim.

Claim 15 recites an integrated circuit having a microprocessor, a set of peripheral devices connected to the microprocessor by a bus, a security module connected to the bus, a communication interface connected to the security module by a dedicated link, a cache memory, and a cache memory controller that writes data to the cache memory in units, each having a length greater than the standard data length of the data processed by the microprocessor, for encryption by the security module. In this particular combination of features, data that is to be encrypted and transferred to an external device, such as a memory, is written into a cache memory in units, e.g. packets, having a length greater than the standard unit length of data processed by the microprocessor, for encryption by the security module.

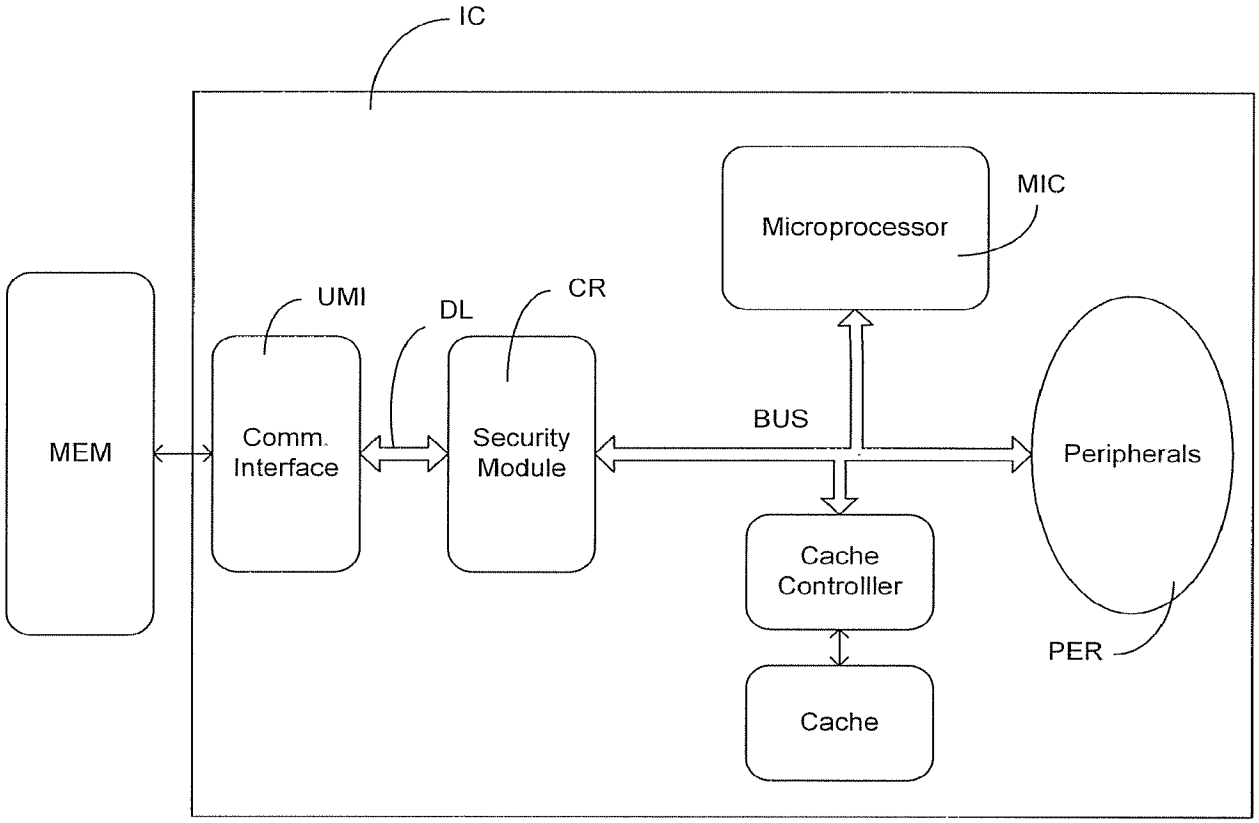
Accordingly, Applicants respectfully request withdrawal of the grounds of rejection, and allowance of claims 12-16.

Respectfully submitted,
BUCHANAN INGERSOLL & ROONEY PC

Date: March 2, 2009

By: /James A. LaBarre/
James A. LaBarre
Registration No. 28632

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620


IC
MIC
Microprocessor
UMI
DL
CR
MEM
Comm.
Interface
Security
Module
BUS
Peripherals
Cache
Controlller
PER
Cache